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| Application Number | 10/761,047 |
| Filing Date | 01/20/2004 |
| First Named Inventor | Stephen R. Van Doren |
| Art Unit | 2457 |
| Examiner Name | Burgess, Barbara N. |

Attorney Docket Number

200313631-1

NON PATENT LITERATURE DOCUMENTS

| | | | |
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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| | | MARTIN, MILO M.K., ET AL., "Token Coherence: Decoupling Performance And Correctness", ISCH-30, pages 1-12, June 9-11, 2003 | |
| | | RAJEEV, JOSHI ET AL., " Checking Cache-Coherence Protocols With TLA+", Kluwer Adademic Publishers, 2003, pages 1-8 | |
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| | | ARCHIBALD ET AL., "Cache Coherence Portocols: Evaluation Using A Multiprocessor Simulation Model", November 1986, ACM Transactions on Computer Systems, Pages 273-298 | |
| | | GHARACHORLOO, KOUROSH ET AL., "Architecture and Design of AlphaServer GS320", Western Research Laboratory, (Date Unknown) | |
| | | GHARACHORLOO, KOUROSH ET AL., "Memory Consistency And Event Ordering In Scalable Shared-Memory Multiprocessors", Computer Systems Laboratory, pages 1-14(Date Unknown) | |
| | | MARTIN ET AL., "Band width Adaptive Snooping", Proceedings Of The Eighth International Symposium On High-Performance Computer Architecture (HPCA'02), 2002 IEEE | |
| | | ACACIO, MANUEL ET AL., "Owner Prediction For Accelerating Cache-to-Cache Transfer Misses In A cc-NUMA Architecture", IEEE 2002 | |
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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